

**A Circuit and Method for Improving Noise Tolerance in Multi-Threaded  
Memory Circuits.**

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**FIELD OF THE INVENTION**

[0001] This invention relates generally to integrated circuit design. More particularly, this invention relates to improving noise tolerance in multi-threaded memory circuits.

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**BACKGROUND OF THE INVENTION**

[0002] In the context of digital circuits, noise is defined as any deviation of a signal from its stable value in those subintervals of time when it should otherwise be stable. Noise in digital circuits can be attributed to several sources such as leakage noise, charge-sharing noise, cross-talk noise, power supply noise, shot noise, thermal noise, and flicker noise. Rigorous noise analysis and noise considerations during design are becoming increasingly important.

[0003] The current capability of a MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is inversely proportional to a MOSFET's length. As a result, more current may be sourced by an individual MOSFET by reducing the length of the MOSFET. However, as the length of a MOSFET is reduced, other problems are created. For example, the threshold voltage may be lowered, resulting in higher levels of leakage current. In addition, leakage current of a MOSFET may introduce noise into a circuit by leaking charge from a node that would ideally retain its initial charge.

[0004] Charge-sharing may be used in a positive manner. DRAMs (Dynamic Random Access Memory) use the principle of charge-sharing to create dense memory devices. DRAMs store an individual data bit by either storing more charge on a capacitor or storing less charge on a capacitor. A DRAM reads data by measuring

the change in voltage on a bitline when the charge on a capacitor is charge-shared with the charge on the bitline. However, unwanted charge-sharing between memory elements may cause correct data stored in a memory element to "flip" to incorrect data.

5           **[0005]** One embodiment of this invention reduces the likelihood that charge-sharing between multi-threaded memory cells will cause incorrect data to be stored in a memory cell. The implementation of this embodiment does not create additional drive fights when the multi-threaded memory cells are written. In addition, charge loss in multi-threaded memory devices due to leakage is reduced by an embodiment  
10 of the invention. A detailed description of one embodiment of this invention is described later.

### **SUMMARY OF THE INVENTION**

15           **[0006]** An embodiment of the invention provides a circuit and method for improving noise tolerance in multi-threaded memory circuits. A PFET is added to the receiving input of each memory cell. The gate of the PFET is connected to the output of the memory cell and the source of the PFET is connected to a control signal of the memory cell. In the case where the dataline is charged near ground by a memory cell  
20 of one thread and a memory cell of another thread, with a high value, is read, noise tolerance is improved by the addition of the PFET to the memory cell.

**[0007]** Other aspects and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the  
25 invention.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

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[0008] Figure 1 is a block diagram of a multi-threaded memory circuit. Prior Art

[0009] Figure 2 is a schematic drawing of a multi-threaded memory circuit. Prior Art

10 [0010] Figure 3 is a block diagram of an embodiment of a multi-threaded memory circuit with improved noise tolerance.

[0011] Figure 4 is a schematic drawing of an embodiment of a multi-threaded memory circuit with improved noise tolerance.

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## **DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT**

[0012] Figure 1 is a block diagram of a multi-threaded memory circuit. Memory cell1, **100**, has an output, **110**, a receiving input, **122**, a control input, **CONTROL3 108** and is connected to **VDD** and **GND**. Memory cell2, **102**, has an output, **112**, a receiving input, **124**, a control input, **CONTROL3, 108** and is connected to **VDD** and **GND**. Transfer gate1, **104**, has an I/O (input/output), **122**, an inputa, **126**, an inputb, **128**, and an I/O, **120**. Transfer gate2, **106**, has an I/O (input/output), **124**, an inputa, **130**, an inputb, **132**, and an I/O, **120**. Receiving input, **122** of memory cell1, **100**, is connected to I/O, **122**, of transfer gate1, **104**. Receiving

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input, **124** of memory cell2, **102**, is connected to I/O, **124**, of transfer gate2, **106**.  
Control signal, **CONTROL1**, **114**, is connected to inputa, **126**, of transfer gate1, **104**  
and to inputb, **132**, of transfer gate2, **106**. Control signal, **CONTROL2**, **116**, is  
connected to inputb, **128**, of transfer gate1, **104** and to inputa, **130**, of transfer gate2,  
5 **106**. A dataline, **120**, is connected to I/O, **120**, of transfer gate1, **104** and transfer  
gate2, **106**.

[0013] One type of noise, charge-sharing, may occur in the multi-threaded  
memory shown in Figure 1. For example, when the dataline, **120**, is charged near  
**GND**, by memory cell2, **102**, the receiving input **122** is held near **VDD**, and transfer  
10 gate1, **104**, briefly connects dataline, **120**, to receiving input **122** to read the value of  
memory cell1, **100**, some charge on receiving input **122** may be transferred to dataline  
**120**. During this time, node **124** is disconnected from dataline, **120**. If enough charge  
is transferred, the "high" value stored on the memory cell1, **100**, may "flip" to a  
"low". If the value stored on the memory cell1, **100** flips to a low from a high, an  
15 incorrect value may be stored on memory cell1, **100**. In this example, only one  
transfer gate is on at any one time.

[0014] Another example of noise due to charge-sharing may occur when the  
dataline, **120**, is charged near **GND**, by memory cell1, **100**, the receiving input **124** is  
held near **VDD**, and transfer gate2, **106**, briefly connects dataline, **120**, to receiving  
20 input **124**, to read the value of memory cell2, **102**. During this time, node **122** is  
disconnected from dataline, **120**. Some charge on receiving input **124** may be  
transferred to dataline **120**. If enough charge is transferred, the "high" value stored on  
the memory cell2, **102**, may "flip" to a "low". If the value stored on the memory  
cell2, **102** flips to a low from a high, an incorrect value may be stored on memory  
25 cell2, **102**. In this example, only one transfer gate is on at any one time.

[0015] Figure 2 is a schematic drawing of a multi-threaded memory circuit.

Memory cell1, **252**, contains PFET, MP1, **200**, with its source connected to **VDD**, its drain, **214**, connected to the gate, **214** of PFET, MP2, **202**, the gate, **214** of NFET, MN2, **206**, and the drain, **214** of NFET MN1, **204**. Memory cell1, **252** also contains  
5 PFET, MP2, **202**, with its source connected to **VDD**, its drain, **216**, connected to the gate, **216** of PFET, MP1, **200**, the gate, **216**, of NFET, MN1, **204**, and the drain, **216** of NFET MN2, **206**. In addition, the source of NFET, MN1, **204** is connected to **GND**. The source **218**, of NFET, MN2, **206**, is connected to the drain, **218**, of NFET, MN3, **208**. The gate, **220**, of NFET, MN3, **208** is connected to CONTROL3, **220** and  
10 the source of NFET, MN3, **208**, is connected to **GND**.

[0016] Memory cell2, **256**, contains PFET, MP4, **226**, with its source connected to **VDD**, its drain, **240**, connected to the gate, **240** of PFET, MP5, **228**, the gate, **240** of NFET, MN6, **232**, and the drain, **240** of NFET MN5, **230**. Memory cell2, **256** also contains PFET, MP5, **228**, with its source connected to **VDD**, its drain,  
15 **242**, connected to the gate, **242** of PFET, MP4, **226**, the gate, **242**, of NFET, MN5, **230**, and the drain, **240** of NFET MN6, **232**. In addition, the source of NFET, MN5, **230** is connected to **GND**. The source **244**, of NFET, MN6, **232**, is connected to the drain, **244**, of NFET, MN7, **234**. The gate, **220**, of NFET, MN7, **234** is connected to CONTROL3, and the source of NFET, MN7, **234**, is connected to **GND**.

20 [0017] Transfer gate1, **254** contains PFET, MP3, **210**, with its source connected to **216**, its drain connected to **250**, and its gate connected to **222**. Transfer gate1, **254** also contains, NFET, MN4, **212**, with its drain connected to **216**, its source connected to **250**, and its gate connected to **224**.

[0018] Transfer gate2, **258** contains PFET, MP6, **236**, with its source  
25 connected to **242**, its drain connected to **250**, and its gate connected to **246**. Transfer

gate2, **258** also contains, NFET, MN8, **238**, with its drain connected to **242**, its source connected to **250**, and its gate connected to **248**.

[0019] One type of noise, charge-sharing, may occur in the multi-threaded memory shown in Figure 2. For example, when the dataline, **250**, is charged near **GND**, by memory cell2, **256**, the receiving input **216** is held near **VDD**, the gate, **222**, of PFET MP3, **210**, is briefly held low, and the gate, **224**, of NFET MN4, **212** is briefly held high to read the value on receiving input, **216**, some charge on receiving input **216** may be transferred to dataline **250**. During this time, node **246** is held high and node **248** is held low. If enough charge is transferred, the high value stored on the memory cell1, **252**, may "flip" to a low. If the value stored on the memory cell1, **252** flips to a low from a high, an incorrect value may be stored on memory cell1, **252**. In this example, only one transfer gate is on at any one time.

[0020] Charge-sharing, may also occur in another way in the multi-threaded memory shown in Figure 2. For example, when the dataline, **250**, is charged near **GND**, by memory cell1, **252**, the receiving input **242** is held near **VDD**, the gate, **246**, of PFET MP6, **236**, is briefly held low, and the gate, **248**, of NFET MN8, **238** is briefly held high to read the value on receiving input, **242**, some charge on receiving input **242** may be transferred to dataline **250**. During this time, node **222** is held high and node **224** is held low. If enough charge is transferred, the high value stored on the memory cell2, **256**, may "flip" to a low. If the value stored on the memory cell2, **256** flips to a low from a high, an incorrect value may be stored on memory cell2, **256**. In this example, only one transfer gate is on at any one time.

[0021] Figure 3 is a block diagram of an embodiment of a multi-threaded memory circuit with improved noise tolerance. Memory cell1, **300**, has an output, **310**, a receiving input, **322**, a control input, CONTROL3, **308** and is connected to

**VDD** and **GND**. Memory cell2, **302**, has an output, **312**, a receiving input, **324**, a control input, **CONTROL3**, **308** and is connected to **VDD** and **GND**. Transfer gate1, **304**, has an I/O (input/output), **322**, an inputa, **326**, an inputb, **328**, and an I/O, **320**. Transfer gate2, **306**, has an I/O (input/output), **324**, an inputa, **330**, an inputb, **332**, and an I/O, **320**. Receiving input, **322** of memory cell1, **300**, is connected to I/O, **322**, of transfer gate1, **304**. Receiving input, **324** of memory cell2, **302**, is connected to I/O, **324**, of transfer gate2, **306**. Control signal, **CONTROL1**, **314**, is connected to inputa, **326**, of transfer gate1, **304** and to inputb, **332**, of transfer gate2, **306**. Control signal, **CONTROL2**, **316**, is connected to inputb, **328**, of transfer gate1, **304** and to inputa, **330**, of transfer gate2, **306**. A dataline, **320**, is connected to an I/O, **320**, of transfer gate1, **304** and transfer gate2, **306**. The source of PFET, MP1, **334**, is connected to **CONTROL3**, **308**. The gate of PFET, MP1, **334**, is connected to the output, **310**, of memory cell1, **300**. The drain of PFET, MP1, **334** is connected to the receiving input, **322**, of memory cell1, **300**. The source of PFET, MP2, **336**, is connected to **CONTROL3**, **308**. The gate of PFET, MP2, **336**, is connected to the output, **312**, of memory cell2, **302**. The drain of PFET, MP2, **336** is connected to the receiving input, **324**, of memory cell1, **302**.

[0022] One type of noise, charge-sharing, is reduced in the multi-threaded memory shown in Figure 3. For example, when the dataline, **320**, is charged near **GND** by memory cell2, **302**, the receiving input **322** is held near **VDD**, and transfer gate1, **304**, briefly connects dataline, **320**, to receiving input **322** to read the value of memory cell1, **300**, some charge on receiving input **322** may be transferred to dataline **320**. During this time, **CONTROL2**, **316** is held high and **CONTROL1**, **314** is held low. The transferred charge is compensated for by the PFET, MP1, **334**. In this case, the voltage on **CONTROL3**, **308**, is near **VDD** and the memory cell1 output, **310** is

near GND. As a consequence, the PFET, MP1, 334, is on and recharges most charge lost to charging-sharing with the dataline, 320. The addition of PFET, MP1, 334, does not introduce any additional drive fights when CONTROL3, 308, is held low.

[0023] Another example of how noise due to charge-sharing may be reduced occurs when the dataline, 320, is charged near GND by memory cell1, 300, the receiving input 324 is held near VDD, and transfer gate2, 306, briefly connects dataline, 320, to receiving input 324 to read the value of memory cell2, 302, some charge on receiving input 324 may be transferred to dataline 320. During this time, CONTROL2, 314 is held high and CONTROL1, 316 is held low. This transferred charge is compensated for by the PFET, MP2, 336. In this case, the voltage on CONTROL3, 308, is near VDD and the memory cell2 output, 312 is near GND. As a consequence, the PFET, MP2, 336, is on and recharges most charge lost to charging-sharing with the dataline, 320. The addition of PFET, MP2, 336, does not introduce any additional drive fights when CONTROL3, 308, is held low.

[0024] Figure 4 is a schematic drawing of one embodiment of a multi-threaded memory circuit with improved noise tolerance. Memory cell1, 452, contains PFET, MP1, 400, with its source connected to VDD, its drain, 414, connected to the gate, 414 of PFET, MP2, 402, the gate, 414 of NFET, MN2, 406, and the drain, 414 of NFET MN1, 404. Memory cell1, 452 also contains PFET, MP2, 402, with its source connected to VDD, its drain, 416, connected to the gate, 416 of PFET, MP1, 400, the gate, 416, of NFET, MN1, 404, and the drain, 416 of NFET MN2, 406. In addition, the source of NFET, MN1, 404 is connected to GND. The source 418, of NFET, MN2, 406, is connected to the drain, 418, of NFET, MN3, 408. The gate, 420, of NFET, MN3, 408 is connected to CONTROL3, 420, and the source of NFET, MN3, 408, is connected to GND.



[0025] Memory cell2, 456, contains PFET, MP4, 426, with its source connected to VDD, its drain, 440, connected to the gate, 440 of PFET, MP5, 428, the gate, 440 of NFET, MN6, 432, and the drain, 440 of NFET MN5, 430. Memory cell2, 256 also contains PFET, MP5, 428, with its source connected to VDD, its drain, 442, connected to the gate, 442 of PFET, MP4, 426, the gate, 442, of NFET, MN5, 430, and the drain, 440 of NFET MN6, 432. In addition, the source of NFET, MN5, 430 is connected to GND. The source 444, of NFET, MN6, 432, is connected to the drain, 444, of NFET, MN7, 434. The gate, 420, of NFET, MN7, 434 is connected to CONTROL3, and the source of NFET, MN7, 434, is connected to GND.

10 [0026] Transfer gate1, 454 contains PFET, MP3, 410, with its source connected to 416, its drain connected to 450, and its gate connected to 422. Transfer gate1, 454 also contains, NFET, MN4, 412, with its drain connected to 416, its source connected to 450, and its gate connected to 424. The source, 420, of PFET, MP7, 452, is connected to CONTROL3. The gate, 414, of PFET, MP7, 452, is connected to  
15 the output of memory cell1, 452. The drain, 416, of PFET, MP7, 452, is connected to the receiving input of memory cell1, 452.

[0027] Transfer gate2, 458 contains PFET, MP6, 436, with its source connected to 442, its drain connected to 450, and its gate connected to 446. Transfer gate2, 458 also contains, NFET, MN8, 438, with its drain connected to 442, its source  
20 connected to 450, and its gate connected to 448. The source, 420, of PFET, MP8, 454, is connected to CONTROL3. The gate, 440, of PFET, MP8, 454, is connected to the output of memory cell2, 456. The drain, 442, of PFET, MP8, 454, is connected to the receiving input of memory cell2, 456.

[0028] One type of noise, charge-sharing, is reduced in the multi-threaded  
25 memory shown in Figure 4. For example, when the dataline, 450, is charged near

GND by memory cell2, 456, the receiving input 416 is held near VDD, the gate, 422, of PFET MP3, 410, is briefly held low, and the gate, 424, of NFET MN4, 412 is briefly held high to read the value on the receiving input, 416, some charge on receiving input 416 may be transferred to dataline 450. During this time, node 446 is held high and node 448 is held low. This transferred charge is compensated for by the PFET, MP7, 452. In this case, the voltage on CONTROL3, 420, is near VDD and the memory cell1 output, 414 is near GND. As a consequence, the PFET, MP7, 452, is on and recharges most of the charge lost to charging-sharing with the dataline, 450. The addition of PFET, MP7, 452, does not introduce any additional drive fights when CONTROL3, 420, is held low.

[0029] Another example of how noise due to charge-sharing may be reduced occurs when the dataline, 450, is charged near GND by memory cell1, 452, the receiving input 442 is held near VDD, the gate, 446, of PFET MP6, 436, is briefly held low, and the gate, 448, of NFET MN8, 438 is briefly held high to read the value on the receiving input, 442, some charge on receiving input 442 may be transferred to dataline 450. During this time, node 422 is held high and node 424 is held low. This transferred charge is compensated for by the PFET, MP8, 454. In this case, the voltage on CONTROL3, 420, is near VDD and the memory cell2 output, 440 is near GND. As a consequence, the PFET, MP8, 454, is on and recharges most of the charge lost to charging-sharing with the dataline, 450. The addition of PFET, MP8, 454, does not introduce any additional drive fights when CONTROL3, 420, is held low.

[0030] The foregoing description of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and other modifications and

variations may be possible in light of the above teachings. The embodiment was chosen and described in order to best explain the principles of the invention and its practical application to thereby enable others skilled in the art to best utilize the invention in various embodiments and various modifications as are suited to the particular use contemplated. It is intended that the appended claims be construed to include other alternative embodiments of the invention except insofar as limited by the prior art.